REMARKS

The following remarks are made in response to the Final Office Action mailed July 26, 2005. Claims 1-24 were rejected. With this Response, no claims have been amended. Claims 1-24 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1-24 under 35 U.S.C. § 102(e) as being anticipated by Arora (U.S. Patent No. 6,393,556).

Applicants submit that the Arora Patent fails to teach or suggest the invention of independent claims 1, 6, 12, 17, and 23.

The Arora Patent discloses changing a privilege level in a processor configured to pipeline instructions. The processor includes a first memory storing an architectural privilege level that is set at a first privilege level, a second memory storing a plurality of instructions, and a pipeline including a plurality of processing stages. A first instruction is fetched from the memory and a determination is made whether the first instruction requires the first privilege level be changed to a second privilege level, and in response thereto, any subsequent instructions are flushed from the pipeline before recording the second privilege level in the first memory. (Abstract).

The processor 30 maintains a "current privilege level" ("CPL") 38 in a memory storage device. The CPL is maintained in the processor's register set. The operating system sets the CPL to prevent the user from performing dangerous or insecure operations. If the pipeline 30 is currently processing an application program instruction, a prior instruction would have set the CPL 38 to the proper privilege level. If an instruction requiring a higher privilege level follows the current instruction, an instruction, such as an "enter privilege code" ("EPC") instruction, that directs the processor to change the privilege level of the CPL must first be processed to increase the privilege level. (Col. 4, lines 13-27).

After decoding an instruction directing the processor to change the CPL 38 from a first to a second privilege level, the processor compares the second privilege level to the CPL 38. (Col. 6, lines 27-31). The processor will compare the CPL 38 with the privilege level

specified in the EPC instruction. If the EPC instruction directs the processor to change the CPL 38 to a higher privilege level, the processor flushes any instructions in the pipeline subsequent to the EPC instruction, and continues processing the EPC instruction. When the EPC instruction is retired, the CPL 38 privilege level is increased. If the EPC instruction specifies a privilege level lower than or the same as the CPL 38, the processor will issue a fault. (Col. 6, lines 46-59).

Applicants submit that the Arora Patent fails to teach or suggest the method of independent claim 1. The Arora Patent fails to teach or suggest **performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level, the privilege promotion instruction including: reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level.**

The Examiner states that the claim 1 limitation of the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level is disclosed by the Arora Patent by "an instruction memory 36 storing a plurality of instructions (storing a privilege promotion instruction in a first page of memory... see Figure 2)." (Office Action, pages 2-3). This claim 1 limitation, however, recites the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level. The Arora Patent does not teach or suggest storing a privileged promotion instruction in a *first page of memory not writeable by application instructions at a first privilege level* as recited in claim 1. The Arora Patent merely discloses that the EPC instruction is fetched from the instruction memory 36. (Col. 4, lines 50-51). The Arora Patent does *not* disclose that the EPC instruction is stored in a first page of instruction memory 36 not writeable by application instructions at a first privilege level.

The Examiner states that the claim 1 limitations of reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level is disclosed in column 6, lines 46-61 of the Arora Patent. (Office Action, pages 2 and 4).

The Examiner also states that "comparing the architectural current privilege level (current privilege level state) with the privilege level of the EPC instruction (previous privilege level state) wherein comparing privilege levels, it is understood that the stored privilege level must be read in the comparison process." (Office Action, page 2). The cited text of the Arora Patent discloses comparing the architectural CPL with the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent fails to disclose the claim 1 limitation of *reading a stored previous privilege level state* and *comparing the read previous privilege level state to the current privilege level.* In the Arora Patent, a previous privilege level state is not stored and therefore cannot be read.

The Arora Patent also discloses that the CPL is compared to the privilege level specified in the EPC instruction. In contrast, claim 1 requires comparing the *read previous privilege level state* to the *current privilege level.* The privilege level of the EPC instruction does not teach or suggest a stored previous privilege level state. Rather, the EPC instruction directs the processor to change the privilege level of the CPL. (Col. 4, lines 24-26). The EPC instruction provides a future privilege level, not a previous privilege level.

The Examiner states that the claim 1 limitation of if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level is disclosed by the Arora Patent in that the Arora Patent discloses "increasing the current privilege level if the privilege level of the EPC is higher than the CPL (Col. 6, lines 46-61)." (Office Action, page 2). The examiner also states that the Arora Patent discloses this limitation by "...increase the architectural current privilege level from privilege level 3 to privilege level 0." (Office Action, page 5). The Arora Patent discloses raising the current architectural CPL to the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent, however, does not disclose the claim 1 limitation of promoting the current privilege level to a second privilege level which is higher than the first privilege level if the previous privilege level state is equal to or less privileged than the current privilege level.

Claim 1 recites if the *previous privilege level state* is equal to or *less privileged* than the *current privilege level*, promoting the current privilege level. In contrast, the Examiner states that the Arora Patent discloses increasing the *current privilege level* if the privilege level of the *CPL* is *lower* than the privilege level of the *EPC*. In addition, the Examiner states

that the privilege level of the EPC instruction discloses the previous privilege level state (Office Action, page 2). Therefore, based on the Examiner's interpretation, claim 1 would recite if the privilege level of the EPC instruction is equal to or less privileged than the current privilege level, promoting the current privilege level. Neither of these two contradictory interpretations of the Arora Patent teaches nor suggests the limitations recited in claim 1.

In view of the above, Applicants believe independent claim 1 to be allowable over the Arora Patent. Dependent claims 2-5 further define patentably distinct independent claim 1. Accordingly, dependent claims 2-5 are also believed to be allowable over the art of record.

Applicants submit that the Arora Patent does not teach or suggest the method of independent claim 6. The Arora Patent fails to disclose **performing a call instruction to a second page of memory not writeable by the application instructions at the first privilege level, the call instruction including: storing the first privilege level in a previous privilege level state; and performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in the second page of memory, the privilege promotion instruction including: reading the stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level.**

For the same reasons as discussed above with reference to independent claim 1, the Arora Patent fails to teach or suggest the limitations of claim 6, which are similar to the above limitations of claim 1.

In view of the above, Applicants believe independent claim 6 to be allowable over the cited reference. Dependent claims 7-11 further define patentably distinct independent claim 6. Accordingly, dependent claims 7-11 are also believed to be allowable over the art of record.

Applicants submit that the Arora Patent does not teach or suggest the computer system of claims 12 or 17 or the computer readable medium of claim 23. Regarding claim 12, the Arora Patent fails to disclose **a memory having a plurality of memory pages including a first memory page storing a privilege promotion instruction, wherein the**

first memory page is not writeable by application instructions at a first privilege level; and **performing the privilege promotion instruction as follows: reads the previous level state; compares the read previously privilege state to the current privilege level; and if the previous privilege level state is equal to or less privilege than the current privilege level, promotes the current privilege level to a second privilege level which is higher than a first privilege level.**

Regarding claim 17, the Arora Patent fails to disclose **a memory having a plurality of memory pages including a first memory page storing application instructions and a second memory page storing a higher privilege routine and a privilege promotion instruction, wherein the second memory page is not writeable by the application instructions at a first privilege level; wherein the processor executes the application instructions with the current privilege level equal to the first privilege level and the application instructions perform a call instruction to the second memory page as follows: stores the first privilege level in a previous privilege level state; and wherein the operating system performs the privilege promotion instruction as follows: reads the stored previous privilege level state; compares the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privilege than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.**

Regarding claim 23, the Arora Patent fails to disclose **reading a stored previous privilege state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a privilege level which is higher than the current privilege level.**

For the same reasons as discussed above with reference to independent claim 1, the Arora Patent fails to teach or suggest the limitations of independent claims 12, 17, and 23, which are similar to the above limitations of claim 1.

In view of the above, Applicants believe independent claims 12, 17, and 23 to be allowable over the cited reference. Dependent claims 13-16 further define patentably distinct independent claim 12. Dependent claims 18-22 further define patentably distinct independent claim 17. Dependent claim 24 further defines patentably distinct independent claim 23.

Accordingly, dependent claims 13-16, 18-22, and 24 are also believed to be allowable over the art of record.

In view of the above, Applicants respectfully request that the rejections to claims 1-24 under 35 U.S.C. § 102(e) be withdrawn and that claims 1-24 be allowed.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-24 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-24 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Response should be directed to either David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854 or Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,

Dale C. Morris et al.,

By their attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2003
Facsimile: (612) 573-2005

Date: 9-26-05
PGB/MAP:bac

Patrick G. Billig
Reg. No. 38,080

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 26 day of Sept., 2005.

By
Name: Patrick G. Billig